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Docket No.: GR 98 P 2191 P

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By: Mark P. Weichselbaum

Date: 5/2/01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Robert Reiner et al.
Applic. No. : 09/771,886
Filed : January 29, 2001
Title : Clocked Integrated Semiconductor Circuit And Method For
Operating Such A Circuit

INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner of Patents and Trademarks,
Washington, D.C. 20231

Sir:

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

Japanese Patent Abstract JP 60 231 285 (Seiki), dated November 16, 1985.

Respectfully submitted,

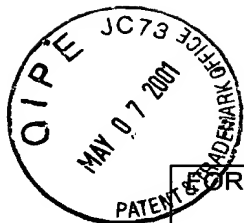
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Date: May 2, 2001

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| FORM PTO-1449 (SUBSTITUTE) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b)) | Attorney Docket No.: GR 98 P 2191 P | Applic. No. 09/771,886 |
| | Applicant Robert Rainer et al. | |
| | Filing Date January 29, 2001 | Group Art Unit |

U.S. PATENT DOCUMENTS

| EXAMINER INITIALS | | PATENT NO. | DATE | PATENTEE | CLASS | SUB CLASS | FILING DATE |
|----------------------|---|------------|------|----------|-------|--------------|----------------|
| | A | | | | | | |
| | B | | | | | | |
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FOREIGN PATENT DOCUMENT

| | | DOCUMENT NO. | DATE | COUNTRY | CLASS | SUB CLASS | TRANSL. YES NO |
|--|---|--------------|----------|---------|-------|--------------|---------------------|
| | J | 60 231 285 | 11/16/85 | Japan | | | X |
| | K | | | | | | |
| | L | | | | | | |
| | M | | | | | | |
| | N | | | | | | |

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

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EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.